CLAIMS:

1. A parallel processing apparatus for processing data based on an instruction word comprising at least two individual instructions used for controlling at least two respective functional units (30-1 to 30-n), said apparatus comprising instruction processing means (40) for processing a first individual instruction extracted from a first instruction word, and at least a second individual instruction extracted from at least a subsequent second instruction word, as a new single instruction word.

2. An apparatus according to claim 1, wherein said instruction processing means (40) is arranged to extract said first and at least second individual instructions if said first and at least second instruction words each comprise one of predetermined instruction patterns with at least one delay instruction, and to compress said first and at least second instruction words into said single instruction word.

3. An apparatus according to claim 2, wherein said delay instruction is a null operation (NOP).

4. An apparatus according to claim 2, wherein said single instruction word is stored in a program memory (50).

5. An apparatus according to claim any one of the preceding claims, wherein said instruction processing means (40) is arranged to add a predetermined control information to said single instruction word, said control information indicating at least one of an allocation of said extracted first and at least second individual instructions to said respective functional units (30-1 to 30-n) and a sequential order of said first and least second individual instructions at their respective functional units.

6. An apparatus according to claim 5, wherein said control information consists of at least one bit added as at least one respective most significant bit to said single instruction word.

7. An apparatus according to claim 5, wherein said instruction processing means (40) is arranged to check said control information in an instruction word read from a program memory (50), to re-establish said first and at least instruction words based on said control information, and to supply said re-established first and at least second instruction words to an instruction decoder (44).

8. An apparatus according to claim 1, wherein said instruction processing means (40) is arranged to mark all instruction words associated with delay slots and branch targets, and to decide on extraction of said first and at least second individual instructions based on the markings.

9. An apparatus according to claim 8, wherein said instruction processing means (40) is arranged to adjust at least one program memory address based on a decided extraction.

10. An apparatus according to claim 1, wherein said parallel processing apparatus is a VLIW processor.

11. A method of decompressing an instruction word comprising at least two individual instructions used for controlling at least two respective functional units (30-1 to 30-n), said method comprising the steps of:

a) checking a control information added to said instruction word;

b) extracting said at least two individual instructions and generating at least two new instruction words each comprising one of said extracted individual instructions, and

c) adding at least one delay instruction to each of said at least two new instruction words,

d) wherein steps b) and c) are performed in response to the result of step a).

12. A method of compressing instruction words each comprising at least two individual instructions used for controlling at least two respective functional units (30-1 to 30-n), said method comprising the steps of:

a) extracting a first individual instruction from a first instruction word;

b) extracting at least a second individual instruction from at least one subsequent second instruction word; and

c) generating from said first and second individual instructions a new single instruction word.

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13. A computer program product comprising code means for controlling a computer system so as to perform the steps of a compression method according to claim 12 or 13 when loaded into said computer system.